REMARKS

In response to the Office Action mailed July 24, 2007, Applicants respectfully request reconsideration. Claims 1 and 13 have been amended herein. As a result, claims 1-36 remain pending for examination with claims 1 and 13 being independent. No new matter has been added.

Rejections Under 35 U.S.C. §103

The Office Action rejected claims 1-36 under 35 U.S.C. 103(a) as being purportedly unpatentable over Pollachek, 4,648,074, in view of Lee et al., 5,909,405, Garni et al., 6,621,729, and Passotti et al., 6,535,428. Applicants respectfully disagree with the rationale behind these rejections and request reconsideration.

1. Clarification of the Rejections of Independent Claims 1 and 13

As a preliminary matter, Applicants note that the Office Action does not point out how all the limitations of claims 1 and 13 are purportedly described by the references. For example, the section of the Office Action that refers to claim 1 (pages 2 and 3) does not address the following limitation of claim 1: "wherein the first load is controlled by the control circuit in response to a voltage of the first conduction terminal of the first load." However, on page 4, the Office Action addresses claims 2-3, 7, 10, 14-18, 23-27 and 33-35 by stating that Garni purportedly describes providing "**the control signal to the gate of PMOS load transistor 14 in response to a drain voltage of the conduction drain of the first PMOS load transistor 14.**" (Emphasis in original). Although the Office Action indicates that certain dependent claims are addressed by this passage, Applicants assume that the Office Action intended this passage to apply to the rejections of independent claims 1 and 13, and not just the referenced dependent claims. Applicants' understanding of the rejections of the independent claims is that claims 1 and 13 are rejected in view of three references: Pollachek, Lee and Garni. If this understanding is incorrect, Applicants respectfully request clarification.

2. Discussion of Cited References

Pollachek

Pollachek's memory circuit operates on the principle of charge and discharge of a bit line and a reference line. FIG. 3 of Pollachek illustrates a memory stack that forms a data storage portion of memory array 30 (Col. 3, lines 43-45). Before the memory stack is read, a bit line is precharged to the voltage V_{DD} by applying a "precharge pulse (PC) to the gate electrode of PT1 which turns PT1 on momentarily" (Col. 3, lines 61-64). In response to receiving the precharge pulse PC, transistor PT1 turns on and the bit line is connected to the supply voltage V_{DD}, and the bit line is charged. Similarly to the charging of the bit line, the reference line is connected to transistor PTR which receives a precharge pulse to turn on the transistor, thus connecting the reference line to the supply voltage V_{DD}. When the bit line and reference line are connected to the supply voltage, the bit line capacitance C1 and the reference line capacitance C2 are charged to a voltage of V_{DD}. After transistors PT1 and PTR are turned off, reference circuit select transistor T_R and word line select transistor WS are turned on so that the data stored in the memory cell can be read by differential sense amplifier 22, based on the respective voltages V_S and V_R provided by the reference and memory cells (Col. 4, line 66 – Col. 5, line 37). Pollachek does not teach or suggest that transistor PTR provides a reading current to a reference cell because reference circuit select transistor T_R is not turned on at the same time as transistor PTR (Col. 5, lines 52-56). As a result, no current path exists through both transistor PTR and the reference cell.

The Office Action states that transistors PT1 and PTR provide load currents I_R and I_S during the period in time in which the first and second PMOS transistors PT1 and PTR are momentarily turned ON by precharge pulses PC. Applicants respectfully disagree. The Office Action appears to assume that the signal and reference currents I_R and I_S must be provided by the transistors PT1 and PTR, but the description of Pollacheck does not support this idea. Quite to the contrary, Pollachek makes it clear that transistors PT1 and PTR are turned off prior to applying current to the reference and memory cells.

The Office Action appears to read the term "current" to cover the charging of capacitor C2 through a first path (i.e., transistor PTR) and the later discharging of capacitor C2 through a different path (i.e., through the sense amplifier and reference cell). Applicants respectfully

disagree with the Office Action's interpretation of the term "current." Although charge can be transferred due to the effect of current, the transfer of charge through paths that are isolated from one another is not a "current." Although various currents flow through Pollachek's circuit, current is not provided from the supply after the path to the supply has been blocked. One of ordinary skill in the art would understand that Pollachek does not intend a current to flow through transistors PT1 and PTR when they are turned off.

Pollachek provides no indication that the current for charging the bit line and reference line is the same as the read currents I_R and I_S. Even if the Office Action considers the term "current" to apply to the situation in Pollachek in which charge is first supplied to capacitor C2 through transistor PTR, then capacitor C2 is later discharged, the total charge supplied by transistors PT1 and PTR is insufficient to provide the read currents I_R and I_S. To the contrary, Pollachek explains that the currents I_R and I_S are established based on the operation of the sense amplifier which amplifies the currents I_R and I_S present on the bit line and reference line (Col. 3, lines 25-30, Col. 7, line 66 – Col. 8, line 21). Thus, although the charge Q provided by transistors PT1 and PTR may be proportional to the charge transferred during readout by currents I_R and I_S, they are not equal to one another because the sense amplifier also contributes to and amplifies currents I_R and I_S.

Although Pollachek describes that transistors PT1 and PTR are turned off prior to reading, the Office Action appears to consider the pre-charge step of Pollachek as being encompassed by the word "reading." However, this interpretation is contrary to Pollachek's description which distinguishes between these two stages (Col. 3 lines 61-64, Col. 5, lines 52-56). There is no indication that Pollachek's use of the word "momentarily" may be interpreted such that the transistors are still turned on even after reading is started. Signal and reference currents I_S and I_R indeed flow through the memory and reference bit lines during reading, but they are not supplied by the transistors PT1 and PTR, which need to be turned off during reading. The circuit of Pollachek would not be able to read a stored bit if the inputs of the differential amplifier 22 (i.e., the bit line and reference line) are connected to V_{DD} during the reading stage.

Garni

Garni describes a differential current sense amplifier for sensing whether a memory bit of a magnetoresistive random access memory is in a high resistance state or a low resistance state. Garni's circuit includes a mid-point reference that is used for distinguishing between the high and low resistance states. FIG. 1 of Garni shows that the symmetric midpoint reference is provided by voltage bias circuit 11. Operational amplifier 12 provides a voltage that is representative of the reference currents through high and low resistance cells (Abstract). This voltage is applied to transistor 22, which supplies a constant reference current to the memory cell with a resistance R_B (Col. 3, lines 43-60). Sense amplifier 10 receives the resulting voltage V_B and determines whether the memory cell is in the high or low resistance state based on V_B. In Garni's circuit, constant sense and reference currents flow through transistors 14, 16, 22, 24 and 26, respectively, and all of these transistors are turned on to read the state of the memory cell.

3. The Combination of Pollachek and Garni is Improper.

As should be appreciated from the above discussion, the principle underlying reading is completely different in Pollachek and Garni. In Pollachek's circuit, reading is based on the measurement of voltage resulting from the discharge of memory and reference bit lines while these lines are isolated form the supply voltage. By contrast, Garni's transistors are turned on during reading to supply a constant current to the reference and memory cells so that the resistance of these cells can be compared. Pollachek's memory cells need to be isolated from the supply during reading, yet Garni's memory cells need to be provided with a constant current during reading.

On page 4, the Office Action states that it would have been obvious to one of ordinary skill in the art to utilize Garni's feedback amplifier as the control circuit of Pollachek to provide the precharge pulse PC to the control gates of both transistors PT and PTR of Pollachek. The Office Action further states that one of ordinary skill in the art would have made such a combination to provide a control bias voltage that is independent of an operating voltage between the source and drain terminals of transistors PT and PTR. Applicants respectfully disagree.

First, the combination proposed in the Office Action would render Pollachek's memory inoperable and thus unsuitable for its intended purpose. As clearly illustrated in FIG. 3 and

described throughout Pollachek, the memory is designed so that transistors PT1 and PTR receive pulses to momentarily turn on these transistors so that the voltage V_{DD} is transferred to the bit line and the reference line. However, Garni's feedback amplifier provides no pulses whatsoever. In stark contrast, Garni's feedback amplifier provides a constant voltage to the control inputs of Garni's transistors so that constant currents are provided to the reference and memory cells. If Pollachek's transistors PTI and PTR were provided with a constant voltage they would not be able to turn on and off as intended. For example, if transistors PT1 and PTR were always turned off, the bit line and reference line would not be charged, and Pollachek's memory could not be read. As another example, if transistors PT1 and PTR were always turned on, then the sense amplifier would always be connected to the supply voltage V_{DD} through both the bit line and the reference line. As a consequence, both the bit line and the reference line would be at the same voltage, thus preventing the sense amplifier from detecting the state of the memory cell.

Second, the Office Action's rationale for combining these references is improper. The Office Action appears to assume that Pollachek's circuit would benefit from using a "control bias voltage independent of an operating voltage" to control transistors PT1 and PTR. This is simply untrue. No matter how stable or supply-independent Garni's reference voltage might have been, one of ordinary skill in the art would not have replaced Pollachek's control pulse with a constant voltage that would render the circuit inoperable. A person of ordinary skill in the art would realize that Pollachek's memory would have to be completely redesigned to function using a constant reference voltage instead of a voltage pulse.

Third, the rationale provided in the Office Action is improper because modifying Pollachek to include Garni's control circuit would completely change the principle of operation of Pollachek's circuit. MPEP 2143.01 requires that the proposed modification cannot change the principle of operation of a reference. As discussed above, Pollachek's read-out is based on the principle that a voltage is initially applied to a bit line, and then the bit line is isolated from the voltage and a differential voltage sensing is performed. The modification suggested in the Office Action would completely change the operation of Pollachek's circuit such that transistor PT1 and PTR would no longer be turned on and off. Instead, a constant voltage would be applied to control these transistors. As discussed above, if these transistors were always turned on, then during readout Pollachek's sense amplifier would no longer be able to sense the difference between the bit line and reference line voltages – instead, these lines would still be connected to

the supply voltage. As a result, the sense amplifier would not be able to produce a meaningful output with both inputs (bit line and reference line) still having the supply voltage applied to them.

In view of the foregoing, the combination of Pollachek and Garni is improper. Accordingly, Applicants respectfully request that this rejection be withdrawn.

4. The Claims Distinguish over the Combination.

Even if the combination of Pollachek and Garni were proper (which it is not), the claims distinguish over the combination. Claim 1 as amended recites, *inter alia*, wherein the reading current passes through both the reference cell and the first load at the same time. The combination of Pollachek and Garni does not teach or suggest this limitation because Pollachek states that the memory cells and reference cells are isolated from the supply voltage by transistor T_R when transistors PT1 and PTR are turned on. As a result, a reading current is not applied to both a reference cell an a load at the same time. Garni fails to remedy this deficiency of Pollachek. Therefore, claim 1 patentably distinguishes over the combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-12 depend from claim 1 and are therefore patentable for at least the same reasons.

Claim 13 as amended recites, *inter alia*, a first transistor having a first conducting terminal coupled to a reference memory cell and a second conducting terminal for connection to a supply voltage, wherein the reading current passes through both the reference memory cell and the first transistor at the same time. As should be appreciated from the above discussion with respect to claim 1, the combination of Garni and Pollachek does not teach or suggest that a reading current passes through both the reference memory cell and the first transistor at the same time. Therefore, claim 13 patentably distinguishes over the combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 14-36 depend from claim 13 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

By: /James H. Morris/
James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000